REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow. Applicant respectfully requests that the foregoing amendments be entered at least because they place the application in condition for allowance.

Claims 1, 7, 13 and 16 are currently being amended. Support for these amendments can be found at least in FIG. 4a and page 8, lines 6-24 of the specification. No new matter has been added.

This amendment changes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1, 3-5 and 7-18 are now pending in this application.

Allowable subject matter

Applicant appreciates the indication that claims 12, 14-15 and 18 are allowed.

Rejections under 35 U.S.C. §§ 102 and 103

Claims 1, 3, 7-9, 11, 13 and 16-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,708,419 to Isaacson et al. ("Isaacson"). Claims 4-5 and 10 were rejected under 35 U.S.C. § 103(a) as being obvious over Isaacson in view of U.S. Patent 4,718,117 to Ma et al. ("Ma"). Applicant respectfully traverses these rejections for at least the following reasons.

Claims 1 and 13

Independent claim 1, as amended, recites "the variable capacitance element being controllable to vary the resonant frequency of the resonant circuit part, wherein the controllable capacitance element is set to have a first capacitance corresponding to a binary 'one' and a second capacitance corresponding to a binary 'zero' for data to be transmitted to the reader, and such that a power transfer from the resonant circuit part of the memory tag to a

resonant circuit part of the reader is substantially the same for both the first capacitance and the second capacitance." This feature is not disclosed in Isaacson.

Isaacson discloses a tag 10 with an IC 14 and resonant circuit 12. The resonant circuit 12 includes a modulation capacitor C_{MOD} and a capacitor C_{ANT}. The IC 14 internally rectifies an induced AC voltage at an ANT input of the IC 14 to provide an internal DC voltage source (col. 4, lines 41-45).

In contrast to claim 1, however, Isaacson does not disclose that its capacitors C_{MOD} and C_{ANT} are "controllable to vary the resonant frequency of the resonant circuit part, wherein the controllable capacitance element is set to have a first capacitance corresponding to a binary 'one' and a second capacitance corresponding to a binary 'zero' for data to be transmitted to the reader, and such that a power transfer from the resonant circuit part of the tag to a resonant circuit part of the reader is substantially the same for both the first capacitance and the second capacitance." Rather, Isaacson discloses that the capacitor C_{MOD} is switched in and out of the resonant circuit 12 to send data pulses to the reader, where the reader senses the changes in consumption of energy to determine the digital data value output from the IC 14 (col. 4, lines 51-62). In other words, the power transfer to the reader in Isaacson would be lower for one type of bit (zero or one) than for another (one or zero). Thus, power transfer to any resonant circuit of the reader in Isaacson would not be substantially the same for both a first capacitance (binary "one") and a second capacitance (binary "zero"). Isaacson fails to anticipate claim 1 for at least this reason.

Independent claim 13 recites "varying the capacitance of the variable capacitance element to have a first capacitance corresponding to a binary 'one' and varying the capacitance of the variable capacitance element to have a second capacitance corresponding to a binary 'zero' for data to be transmitted to the reader, and such that a power transfer from the resonant circuit part of the tag to a resonant circuit part of the reader is substantially the same for both the first capacitance and the second capacitance", and thus is not anticipated by Isaacson for reasons analogous to claim 1.

Claims 7 and 16

Independent claim 7, as amended, recites "the variable capacitance element being controllable to vary the resonant frequency of the resonant circuit part, wherein the controllable capacitance element is set to have a first capacitance corresponding to a binary 'one' and a second capacitance corresponding to a binary 'zero' for data to be transmitted to the reader, the first capacitance corresponding to a resonant frequency of the resonant circuit part of the memory tag slightly detuned from a resonant frequency of a resonant circuit part of the reader in a first direction, the second capacitance corresponding to a resonant frequency of the resonant circuit part of the memory tag slightly detuned from a resonant frequency of a resonant circuit part of the reader in a second direction opposite to the first direction." Thus, in claim 7, the tag resonant circuit resonant frequency for the first capacitance (binary "one") is detuned from the reader resonant frequency in one way, while the tag resonant circuit resonant frequency for the second capacitance (binary "zero") is detuned in the opposite way. This feature is not disclosed by Isaacson.

Rather, in Isaacson the resonant circuit of the tag is switched in and out of resonance with the reader during data transfer (See col. 4, lines 51-62). In this case the capacitance of the resonant circuit 12 of Isaacson would be switched between detuning and being in resonance with the resonant circuit of the reader during data transfer. In other words, either a binary "one" or a binary "zero" would correspond to the situation where the resonant circuits of the tag and reader are in tune with each other.

Independent claim 16 recites "varying the capacitance of the variable capacitance element to have a first capacitance corresponding to a binary 'one' and varying the capacitance of the variable capacitance element to have a second capacitance corresponding to a binary 'zero' for data to be transmitted to the reader, the first capacitance corresponding to a resonant frequency of the resonant circuit part of the memory tag slightly detuned from a resonant frequency of a resonant circuit part of the reader in a first direction, the second capacitance corresponding to a resonant frequency of the resonant circuit part of the memory tag slightly detuned from a resonant frequency of a resonant circuit part of the reader in a

second direction opposite to the first direction", and thus is not anticipated by Isaacson for reasons analogous to claim 7.

Ma was cited for disclosing details of a varactor diode, but fails to cure the deficiencies of Isaacson.

The dependent claims are patentable for at least the same reasons as their respective independent claims, as well as for further patentable features recited therein.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date: July 10, 2006 By _____

HEWLETT-PACKARD COMPANY
Customer No.: 022879

William T. Ellis
Attorney for Applicant
Registration No. 26,874

Thomas G. Bilodeau
Attorney for Applicant
Registration No. 43,438